REMARKS

Claims 1 to 19 were pending in the application at the time of examination. Claims 1 to 19 stand rejected as obvious.

Claims 1 to 5, and 11 to 19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,659,690, hereinafter Stuber, in view of knowledge commonly known in the art as evidenced by the Free On-Line Dictionary of Computing.

Applicant respectfully traverses the obviousness rejection. Applicant notes that even though the claims were not amended, a new basis for the combination of references was presented for the first time in the final office action. This is effectively a new grounds of rejection because the motivation for the combination of references has been changed. Accordingly, this action should not have been made final. Applicant respectfully requests withdrawal of the designation of the final designation of the pending office action.

In the first action, the rationale for combining references in the rejection of Claim 1 was stated as:

> . . . in order to increase the available memory space by moving infrequently used I/O control blocks from the main memory to a secondary memory . . ., as well as to reduce the bottlenecks that can occur by having only four active control blocks.

Paper No. 2, page 4.

In the final action, the rationale for combining references in the rejection of Claim 1 was stated as:

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> . . . in order to extend the addressing capability and allow storage of multiple objects on each page, thus allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available.

Paper No. 4, page 3.

No citations to the prior art were given in either motivation.

Applicant respectfully submits that the stated motivation fails to comply with the requirements of the MPEP and is inconsistent with the level of skill in the art. First, the MPEP directs:

> 2143.01 Suggestion or Motivation To Modify the References [R-2]
>
> THE PRIOR ART MUST SUGGEST THE DESIRABILITY OF THE CLAIMED INVENTION
>
> "There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art."

MPEP §2143.01, 8th Edition, Rev. 2, p. 2100-129 (May 2004).

As examination of each of those possible sources for the motivation shows that the above quoted motivation is not based upon a source permitted by the MPEP.

As stated in the motivation, the nature of the problem to be solved is "allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available." As discussed more completely below, this motivation is unrelated to Applicant's invention as the invention increases the amount of physical memory available in array. Therefore, the motivation fails to address "the nature of the problem to be solved."

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The teachings of the prior art explicitly demonstrate "allowing more control blocks to be present in the control block array." Specifically, Applicant notes that the primary reference, Stuber, teaches a four slot SCB array, where each SCB was referred to a page, i.e., "Each page represents one SCB." Stuber, Col. 18, lines 42 and 43. The admitted prior art in the instant application stated, " The prior art SCB array had 255 storage sites available." Specification, Page 2, lines 13 and 14. Thus, one of skill in knew how to increase the SCB array of Stuber from a four site array to a 255 site array.

Thus, the prior art taught how to increase the size of a SCB array for a host adapter, and so this motivation was known and would teach away from the motivation given by the Examiner. Therefore, the teachings from the prior art do not support the stated motivation.

The general knowledge of paging cited by the Examiner fails to suggest anything concerning a hardware I/O control block array for a parallel SCSI host adapter. The general knowledge on paging is not concerned with a parallel SCSI host adapter or with a hardware control block array for a parallel SCSI host adapter. In fact, the newly cited prior art taught that a particular operating system of dedicated hardware i.e., a MMU, were required to support paging. None of the cited prior art contemplates the inclusion of such structures in a parallel SCSI host adapter. Moreover, the pages of interest are those physically in the SCB array and not some scheme to roll pages in and out of memory so that a larger memory space and the physical memory space available can be utilized. Thus, the last MPEP criterion is not satisfied by the above quoted motivation.

In the three additional references cited by the Examiner, Bradley stated "This invention relates to . . . the method for accessing an amount of memory greater than can be normally

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accessed using a given size address bus." Bradley, Col. 1, lines 5 to 8. De Sanna stated "A memory management unit . . . allocates space in a memory unit. . . . to a number of user tasks being performed concurrently by a CPU." De Sanna, Abstract. Sexton et al. taught "Memory management information about the page is stored in a page header at the beginning of the page, while the remaining space of the page is devoted for storing objects." Sexton et al., Abstract.

Thus, the level of skill as evidenced by this newly cited prior art teaches paging is used for accessing memory greater than can normally be accessed, is used to support user tasks being performed concurrently by a CPU, and a specialized page structure to facilitate memory management. This knowledge adds nothing to the basic knowledge of paging and in fact is associated in each instance with expanding the memory space beyond the physical memory space, which is unrelated to Applicant's invention.

Finally, the Examiner's rationale for the modification mischaracterizes Applicant's invention as recited in the Claims. The Examiner's basis was "allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available." As recited in the claims and shown in the drawings, the physical memory is increased, and so the Examiner's very motivation teaches away from Applicant's invention.

Moreover, it is well known in the field of SCSI host adapters that on-board memory space, and in particular, the memory space available for the firmware used to control the host adapter sequencer is very limited. For example, in Stuber, it was taught how to build a specialized RISC processor and an instruction set used in the firmware based upon the silicon space available in a host adapter. This knowledge of limited available storage space for firmware and how to increase the number of storage spaces in a SCB array must be

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considered in determining the level-of-skill in the art that is based upon the cited prior art. Based upon this knowledge, those of skill would not be motivated to incorporate the complex operating systems and hardware shown in the prior art, relied upon by the Examiner, into a host adapter.

In addition, the improper motivation, the rejection fails to consider the claims as a whole as required by the MPEP for an obviousness rejection. The MPEP directs:

> "[A] claim preamble has the import that the claim as a whole suggests for it." *Bell Communications Research, Inc. v. Vitalink Communications Corp.*, 55 F.3d 615, 620, 34 USPQ2d 1816, 1820 (Fed. Cir. 1995). "If the claim preamble, when read in the context of the entire claim, recites limitations of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim."

MPEP § 2111.02, 8th Edition, Rev. 2, p. 2100-50 (May 2004).

Claim 1 recites:

> A method for accessing hardware I/O control blocks, which are stored in an hardware I/O control block array, by a parallel SCSI host adapter, (Emphasis Added.)

Thus, the method is for accessing hardware I/O control blocks stored in a hardware I/O control block array and not for I/O control blocks stored in some other location and moving the blocks between the two locations. The explicit claim language shows that the stated motivation fails to consider the claims as a whole as required by the MPEP in an obviousness rejection.

The method goes on to explicitly define how the blocks are stored in "one page of a plurality of pages of said . . . array." Thus, the array includes the plurality of pages and so as stated above this is directly contrary to the stated motivation, which is further evidence that explicit claim limitations have not been considered.

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It is expressly recited in the Claims that the plurality of pages is included within the array. Accordingly, the motivation to use paging based upon the rationale in the prior art is unrelated to Applicant's invention as recited in Claim 1.

The MPEP further directs:

> FACT THAT REFERENCES CAN BE COMBINED OR MODIFIED IS NOT SUFFICIENT TO ESTABLISH *PRIMA FACIE* OBVIOUSNESS
>
> The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.

MPEP §2143.01, 8th Edition, Rev. 2, p. 2100-131 (May 2004).

The prior art does not suggest any reason to use paging because the pages are not being swapped in and out of the array based on usage to allow the total memory requirements to exceed the capacity of the array. Applicant further points out that a new use of a known structure is one of criterion for patentable subject matter. In fact, using paging to expand the available memory beyond the physical memory teaches away from using paging in a situation where the total memory requirements are met as in Claim 1.

Finally, Applicant notes that the Examiner dismisses the inherent properties of Applicant's invention as disclosed in the specification. The Examiner's comments are in direct contradiction of the requirements of the MPEP and show that a proper "as a whole inquiry" has not been done on multiple levels. The explicit statements in the specification of the properties include:

> With expanded SCB array 110, all SCSI target addresses can be supported at the same time. There is no restriction on how SCSI bus 180 is populated with target devices. No portion of array 110 is allocated to a

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particular SCSI target to the exclusion of other SCSI target devices. No special hardware assistance is required to access a SCB by a reconnecting target device. Sequencer 150 performs the search.

Description, page 15, line 26 to page 16, line 2.

For the Examiner to say that these are "merely possibilities" suggests that it could be done in another way. However, the Examiner has provided no basis for stating that not all SCSI target addresses can be supported at the same time. The Examiner has not explained how restrictions on how the SCSI bus is populated with target devices would be supported by the present invention. The Examiner has not shown how allocating a portion of the array to a particular SCSI target to the exclusion of other SCSI target devices would work. The remarks are unsupported by any citations or facts. Accordingly, this is an inappropriate rationale for ignoring the specific requirements of the MPEP with respect to inherent properties and for ignoring the explicit statements in the MPEP, and in the disclosure.

Any one of the above facts is sufficient to overcome the obviousness rejection. Accordingly, Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 1.

With respect to the obviousness rejection of Claims 2 to 5, the Examiner relied upon the same motivation to combine the references as noted above. Therefore, the above comments with respect to Claim 1 and the combination of references are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of each of Claims 2 to 5.

With respect to Claim 11, the Examiner used the same motivation to combine the same references as discussed in Claim 1. However, as noted above and incorporated herein by reference, the hardware I/O control blocks are expressly stated

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to be "stored in a hardware I/O control block array." There is no recitation or description of "allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available." Therefore, the above comments with respect to Claim 1 are directly applicable and are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 11.

With respect to the obviousness rejection of Claims 13 to 15, the Examiner relied upon the same motivation to combine the references as noted above for Claim 11. Therefore, the above comments with respect to Claim 11 and the combination of references are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of each of Claims 13 to 15.

With respect to Claim 16, the Examiner used the same motivation to combine the same references as discussed in Claim 1. However, as noted above and incorporated herein by reference, the hardware control blocks are expressly stated to be "in a memory." There is no recitation or description of "allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available." In addition, the memory is expressly stated to include "a paged hardware I/O control block array," and then the array is further expresaly defined. Therefore, the above comments with respect to Claim 1 are directly applicable and are incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 16.

With respect to the obviousness rejection of Claims 17 to 18, the Examiner relied upon the same motivation to combine the references as noted above for Claim 16. Therefore, the above comments with respect to Claim 16 and the combination of references are incorporated herein by reference. Applicant

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requests reconsideration and withdrawal of the obviousness rejection of each of Claims 17 to 18.

With respect to Claim 19, the Examiner used the same motivation to combine the same references as discussed in Claim 1. However, as noted above and incorporated herein by reference, the expanded SCSI control block array includes the recited storage sites. There is no recitation or description of "allowing more control blocks to be present in the control block array while not increasing the amount of physical memory available." Therefore, the above comments with respect to Claim 1 are directly applicable and are incorporated herein by reference. Moreover, Applicant has not used "SCSI I/O control block," and "SCSI I/O control block storage site" interchangeably. The two are different. A SCSI I/O control block is stored in a storage site, but a storage site may or may not store a SCSI I/O control block. Claim 19 does not recite "SCSI hardware control blocks." Therefore, to use the two interchangeably as suggested by the Examiner is error. Applicant requests reconsideration and withdrawal of the obviousness rejection of Claim 19.

In the rejection of Claim 6 that includes the limitations of Claims 1, 3, 4, 5, and 6, the Examiner relied upon a combination of Stuber and Lysinger. The Examiner has modified the teachings of all the references without explaining how the modifications would work.

Lysinger is concerned with only values in rows of the array and does not consider a paged array. Lysinger changes a value of a counter to address row by row in the array until a match is found in a row. Lysinger teaches a single counter that addresses the entire contents of the array. This is fundamentally different from what Applicant recites in Claim 6.

Applicant does not recite walking the array as stated by the Examiner, but rather selectively testing data a storage site in each page of the array until a match is found.

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Applicant does not address every row in the array. Thus, the Examiner must selectively modify Lysinger and selectively modify Stuber. In addition, the Examiner's rejection again mischaracterizes the express limitations recited in the claim. Accordingly, the obviousness rejection of Claim 6 is not well founded for multiple reasons. Applicant respectfully requests reconsideration and withdrawal of the obviousness rejection of Claim 6.

Claims 7 to 10 depend from Claim 6. Therefore, assuming the additional information cited by the Examiner is properly combined, the additional information does not overcome the deficiency in the rejection with respect to Claims 1, 4 and 6 as noted above and incorporated herein by reference. Applicant requests reconsideration and withdrawal of the obviousness rejection of each of Claims 7 to 10.

Claims 1 to 19 remain in the application. For the foregoing reasons, Applicant(s) respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF TRANSMISSION
I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office, Fax No. (703) 872-9306, on the date shown below.

Jan O' Dell — August 26, 2004
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Respectfully submitted,

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